Claim Objections

Claims 7 and 16 were objected to under 37 C.F.R. 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.

Claims 6, 7, 13 and 16 were all amended to respond to the objections.

Claim 1 was objected to because of the following informalities: in line 2 of claim 1, the phrase "clock signals" should be deleted.

The amendment to claim 1 is responsive to the objection to that claim.

Claim 20 was objected to because of the following informalities: In line 9 of claim 20, the word "shift" should be replaced with the word "lock".

The amendment to claim 20 is responsive to the objection of that claim and incorporates the suggested correction.

None of the amendments made in response to the objections stated in the Office Action were made for the purpose of responding to a rejection based upon the patentability of those claims within the meaning of *Festo Corp. v Shoketsu Kinzoku Kogyo Kabushiki Co.* 234 F.3d 558 (Fed. Cir. (2000) (en banc), *cert. granted* 121 S. Ct. 2519 (2001).

§102 Rejection of the Claims

Claims 1 and 4-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Li et al. (U.S. Patent No. 5,058,132).

The cited Li et al patent relates to a clock distribution system which receives a reference clock signal in a clock distribution device and generates a high frequency clock signal and a plurality of local clock signals separated by a phase which is selected by a SEL PHASE signal which is fed into the clock distribution device. The Li et al patent does not show a circuit for dividing a clock signal into N clock signals having a relative phase separation of 360°/2N using a Johnson counter having N stages. As shown in the waveform illustrations of Fig. 6a and 6b of Li, the 8ns/16/ns SEL PHASE signal, which is delivered to the Johnson counter 114 in Fig. 2,

delays each of the LBC1 through LBC5 signals from the Johnson counter 114 by a specific and selectable time delay (either 8 or 16ns) rather than causing a phase shift that is fixed even if the input clock signal is varied in frequency.

"Phase shift" and "time delay" between periodic waveforms are not equivalent as the frequency of the waveforms is varied. A constant time delay results in a constant phase shift only when the frequency of the waveform remains constant. The Li et al circuit provides time shifted signals on outputs LBC1 through LBC5 (as Fig. 6a and 6b clearly show) rather than phase shifted output signals.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Claim 1 recites: "a Johnson counter having N stages ... providing at least two output signals from at least two of the N stages of the Johnson counter as clock signals each having a phase displaced from the phase of the other by 360/2N°" In contrast, the cited Li et al patent shows a clock distribution device 100 where the output signals LBC1 through LBC 5 from the stages of the Johnson Counter are shifted from each other by a selected one of two predetermined, fixed, time delays (See Figs. 6a and 6b) which are described in Li et al as being determined by the SEL PHASE signal shown in Fig. 2 of the cited Li et al patent. Since the Li et al patent shows a circuit where the shift between the signals is a fixed time delay rather than a fixed phase angle of 360/2N°, as claimed in claim 1; an angle which is independent of the clock frequency. Thus, the Li et al patent does not teach each element of claim 1.

Claim 4 now recites that the output signals from the counter each have having a phase "displaced from the phase of the input signal by a fixed angle". In contrast, the Li et al patent

shows a circuit where the signals are delayed by a fixed amount relative to each other, independently of the clock frequency, rather than displaced in phase from the input clock signal. Thus, the Li et al patent does not teach each element of claim 4.

Claim 6, which was amended in response to an objection as explained above and not for purposes of patentability, recites the plurality of clock signals are "phase shifted from the clock signal by fixed angular increments". In contrast, the Li et al patent shows a circuit where the signals are delayed by a fixed amount relative to each other. Thus, the Li et al patent does not teach each element of claim 6.

Claims 11 and 12 have been canceled.

Claim 13, which was amended in response to an objection as explained above and not for purposes of patentability, calls for the multistage counting circuit to provide a plurality of clock signals "phase shifted from the (input) clock signal". In Li et al, the signals are time delayed from each other rather than phase shifted. Thus the Li et al patent does not teach every element of claim 13.

Claim 20 calls for a method which provides phase shifted clock outputs from the Johnson counter. The Li et al patent shows outputs which are time delayed with respect to each other rather than phase shifted. Thus the Li et al patent does not show every element of claim 20.

Reconsideration of independent claims 1, 4, 6, 13 and 20 is respectfully requested in view of the above. Dependent claims 2-5, 7-9, 12, 14-17, 19 and 21 are also allowable over Li et al since they each show further features additional features to those of the independent claims which, as indicated above, are believed to be patentable over Li et al.

Claims 1 and 4-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Fuji (U.S. Patent No. 5,315,269).

The cited Fuji et al patent is for a phase locked loop circuit having first and second "frequency demultipliers" which are referred to, in the specification as "Johnson counters". The embodiment in Fuji et al which is relied upon in support of the rejection requires two Johnson counters, a voltage controlled oscillator, and additional circuitry.

Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation because Fuji et al does not teach each and every claim element. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991).

In claim 1 the phase lock loop circuit is receiving "an input signal having a frequency Fo and providing an output signal having a frequency 2NFo". In contrast, in Fig. 7 of Fuji et al, the input signal IN and the output signal OUT both have the same frequency (see chart in Fig. 10).

Claim 1 also calls for a Johnson counter connected to receive as an input the output signal of the phase lock loop circuit and "providing an output signal as an error signal to the phase lock loop circuit". Neither the first nor the second Johnson counter {frequency demultiplier (104 or 105)} of Fuji et al receives as an input the output signal of the phase lock loop circuit AND provides "an output signal as an error signal to the phase lock loop circuit" as claim 1 requires. The signal 106 provided to the phase lock loop in Fig. 7 of Fuji is not one of the output signals 71, 72, 73 and 74 of Fig. 7 as can be seen in the waveform illustrations of Fig. 10. Thus the Fuji patent does not teach every element of claim 1.

Claim 4 recites that the multi-stage counter receives as an input signal the output of the phase lock loop circuit and provides "clock signals each having a phase displaced from the phase of the input signal (to the phase lock loop) by a fixed angle". In Fuji, second frequency demultiplier 105 is a Johnson counter receiving as an input the OUT signal from the phase lock loop. It does not provide "clock signals each having a phase displaced from the phase of the input signal" because the input signal IN in Fuji does not even have the same frequency as the clock signals 71, 72, 73, and 74 of second frequency demultiplier 105. It is also not providing an error signal to the phase lock loop circuit" as claim 4 requires. Thus the Fuji et al patent does not teach each element of claim 4.

Claim 6 calls for a "multistage counting circuit to provide a plurality of clock signals at the frequency of the input clock signal". In Fuji, as can be seen from the waveforms of Figs. 6a and

6b, the signals 71, 72, 73, and 74 from the second frequency demultiplier 105 are not at the same frequency as the input clock signal IN as claim 6 requires. Thus the Fuji et al patent does not teach each element of claim 6.

Claims 11 and 12 have been canceled.

Claim 13 calls for a phase detector for comparing an input clock signal to an a feedback signal provided by the multiphase counting circuit. In Fuji et al, the input clock signal IN is not compared to the feedback signal provided by the multistage counter 105. Thus the Fuji et al patent does not teach each element of claim 13.

Claim 20 calls for "applying a clock signal to a signal input of a phase lock loop circuit". In Fuji et al the input clock signal IN is not applied to the signal input of the phase lock loop circuit and compared to the output of the Johnson counter as claim 20 requires. Thus the Fuji et al patent does not teach every element of claim 20.

Reconsideration of independent claims 1, 4, 6, 13 and 20 is respectfully requested in view of the above. Dependent claims 2-5, 7-9, 12, 14-17, 19 and 21 are also allowable over Fuji et al since they each show features additional to those of the independent claims which, as explained above are believed to be patentable over Fuji.

§103 Rejection of the Claims

Claims 2-3 and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fuji (U.S. Patent No. 5,315,269).

The Office Action rejected claims 2-3 and 21 based on Fuji. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the rejected claims on found in Fuji. Since all the elements of the rejected claims are not found in Fuji, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

Claims 2-3 and 21 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Li (U.S. Patent No. 5,058,132) in view of Fuji et al (U.S. Patent No. 5,315,269).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Applicant traverses the rejection based upon a combination of Li et al and Fuji on the grounds that the Office Action, in failing to establish that there is a suggestion or motivation to alter or combine the Li et al and Fuji patents, fails to establish a prima face case of obviousness, since the Office Action fails to meet the requirements of *M.P.E.P.* § 2142 imposed on the Patent Office in *Fine.*

Reconsideration and allowance of claims 2-3 and 21 is respectfully requested.

Double Patenting Rejection

Applicant is advised that should claim 8 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof.

Applicant is advised that should claim 15 be found allowable, claim 18 will be objected to under 37 CFR 1.375 as being the substantial duplicate thereof.

Claims 10 and 18 have been cancelled without prejudice. Since claims 8 and 15 are drawn to the same invention as cancelled claims 10 and 18, their cancellation is not made for the purpose of responding to a rejection based upon the patentability of those claims within the meaning of *Festo Corp. v Shoketsu Kinzoku Kogyo Kabushiki Co., supra.*

Conclusi n

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 612-6970 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 22 day of February, 2002.

Name _____ Signature _____